



(43) **Pub. Date:** **Jan. 16, 2020**

This cross-sectional view illustrates a semiconductor device. The substrate consists of several layers: a bottom n-type layer (7), a p-type layer (9), and four stacked p-type layers (8a, 8b, 8c, 8d). Two transistor structures, TX1 and TX2, are formed on the surface. TX1 includes a gate stack (31, 33, 32) and a contact (11). TX2 includes a gate stack (41, 42) and a contact (12). A dashed line X3 indicates a cross-section A-A' through the device. Other regions are labeled with n, p, p+, and n+ to denote their semiconductor type.

FIG. 1

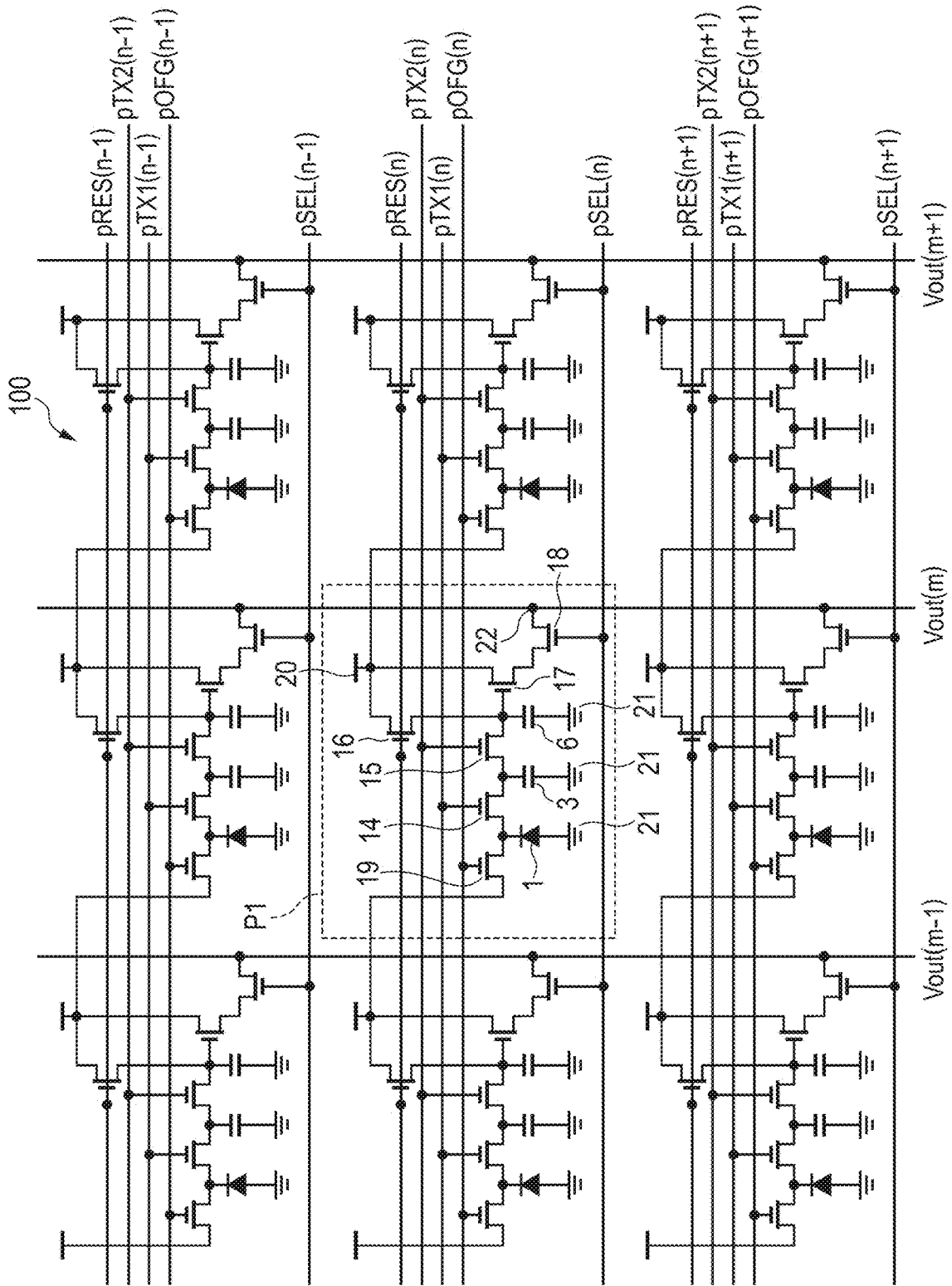
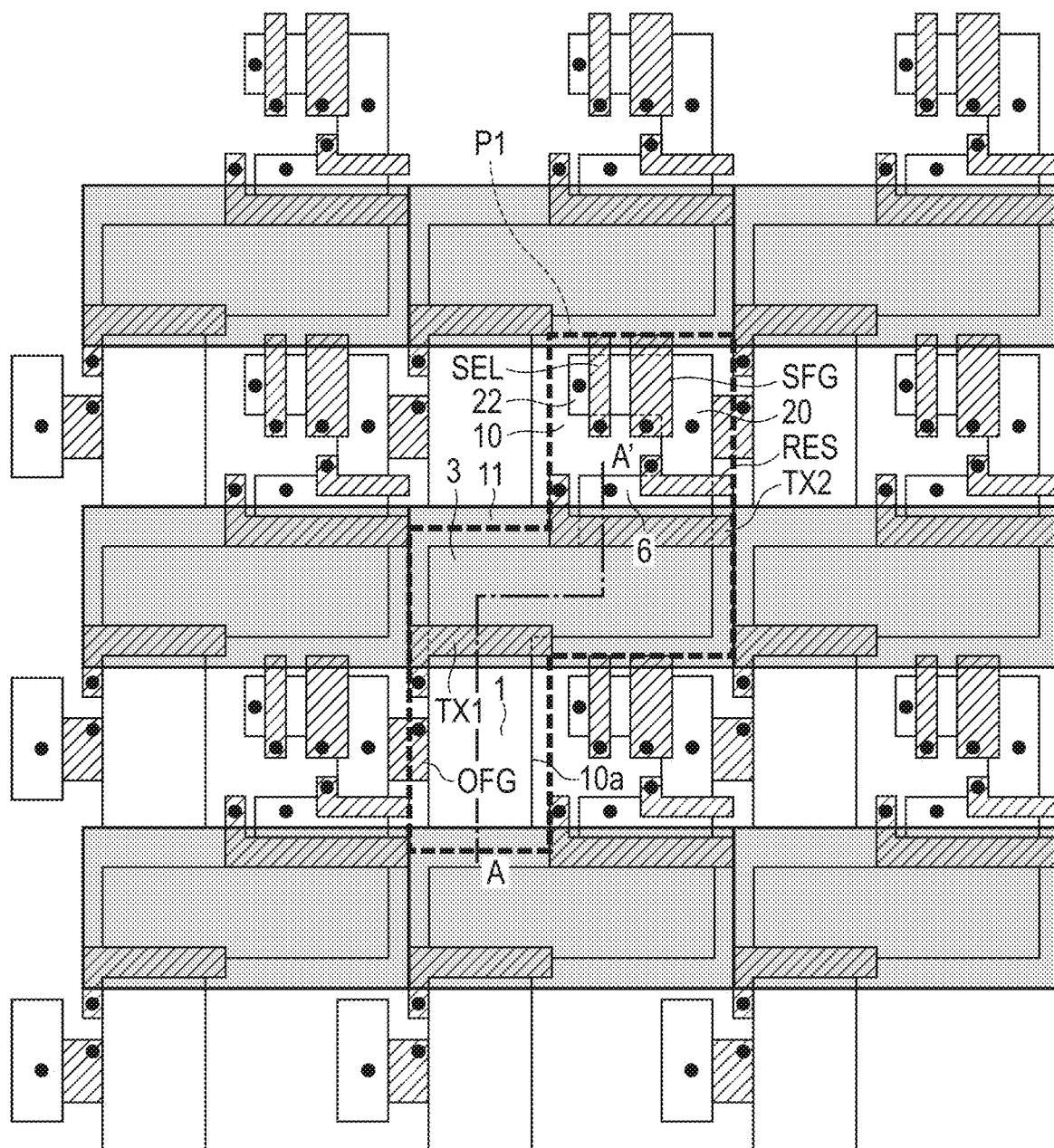


FIG. 2



The diagram is a cross-sectional view of a semiconductor device. At the bottom is a substrate (7) with an n-type region (9). Above this is a p-type layer (p). A stack of four p-type layers (8a, 8b, 8c, 8d) is shown, collectively labeled as 8. Above these layers is an n-type region (n). The device is bounded by regions A and A' on the left and right. Two transistors, TX1 and TX2, are shown. TX1 has a gate stack (3) with layers 41 and 42, and a source/drain region (6). TX2 has a gate stack (3) with layers 41 and 42, and a source/drain region (6). A central region (5) is shown with a gate stack (3) and a source/drain region (6). The device is also labeled with 10, 11, 12, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100.

FIG. 6

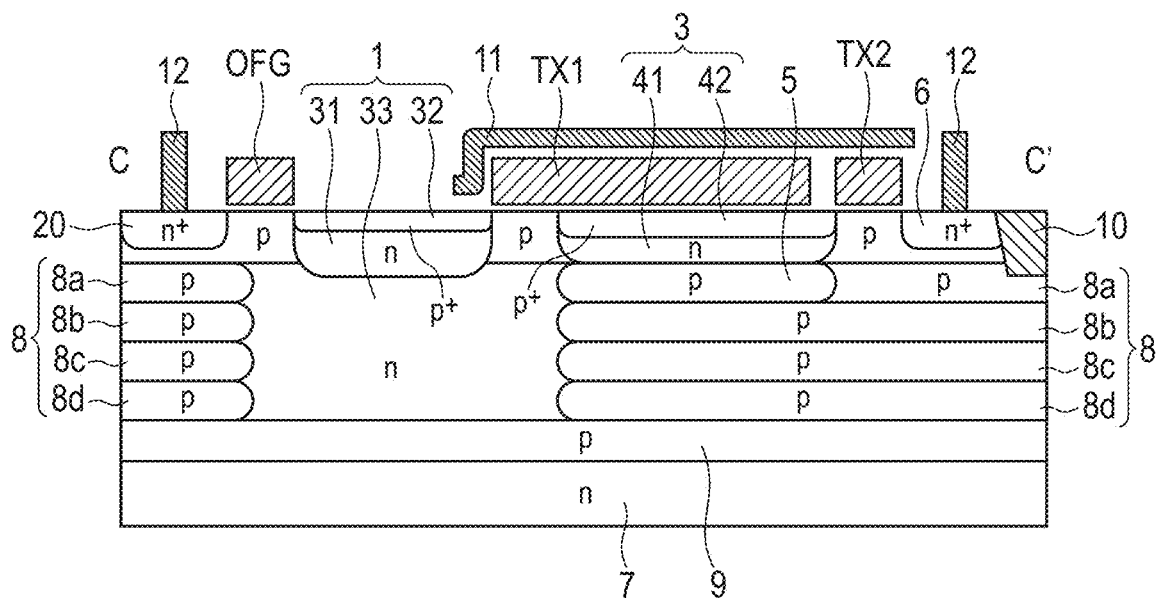


FIG. 7

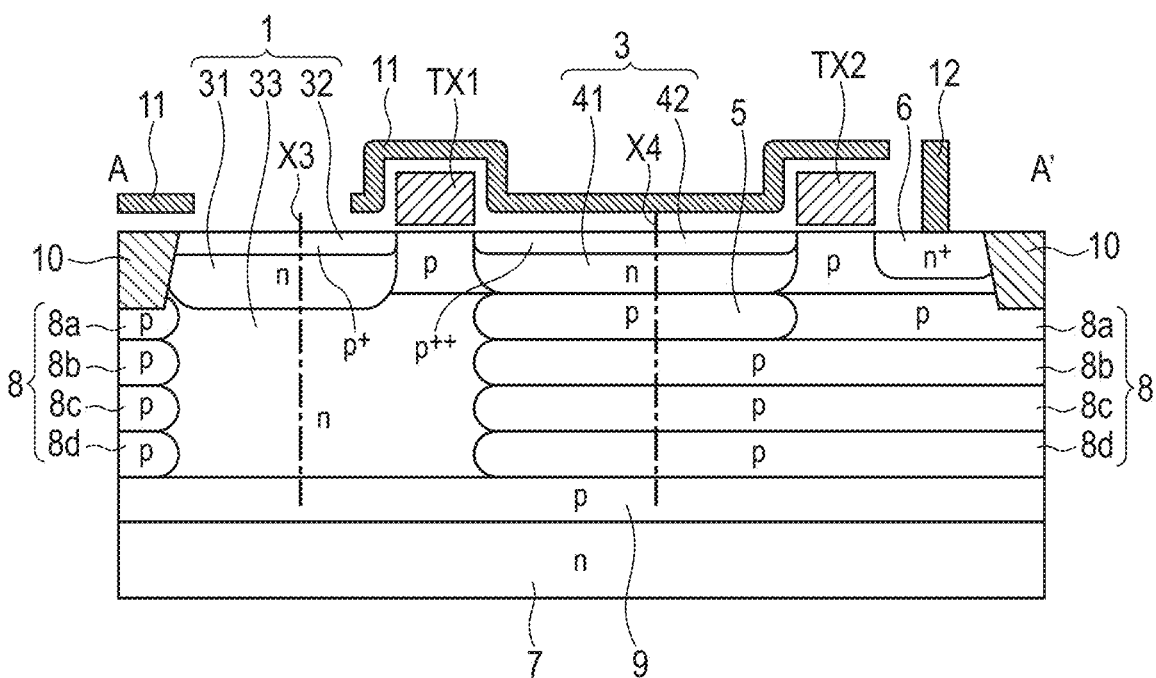


FIG. 8

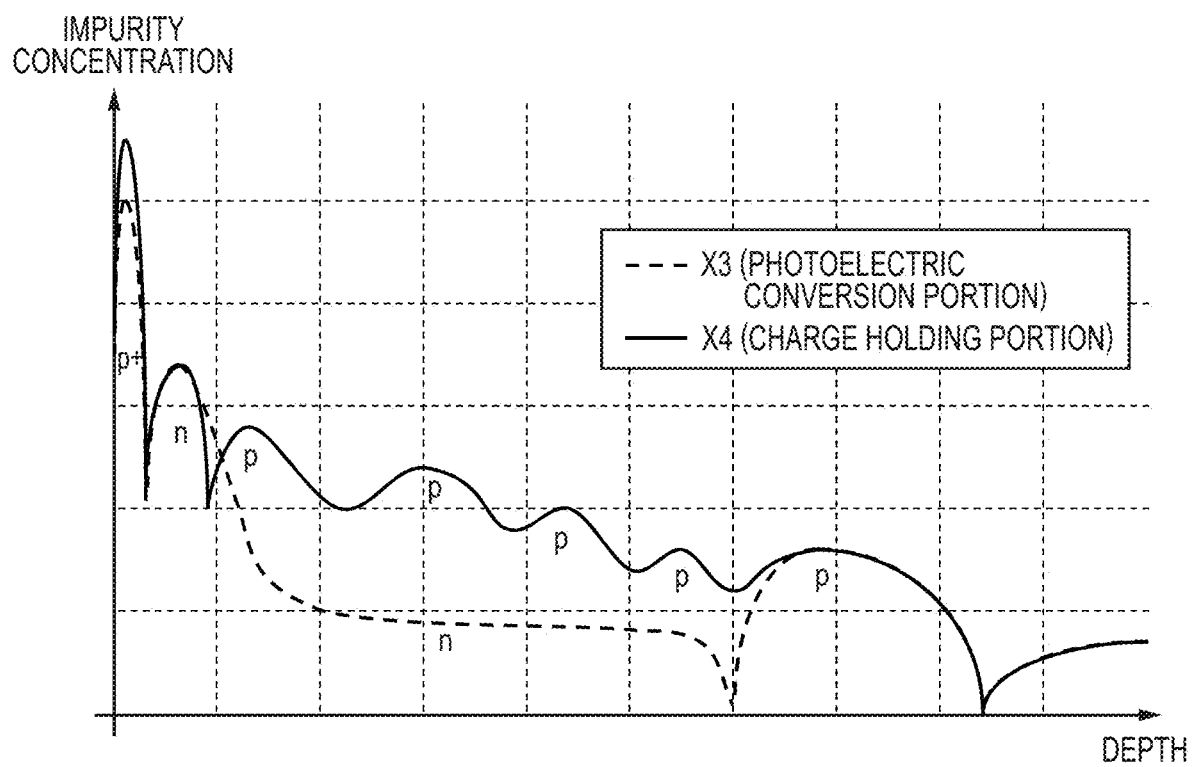


FIG. 9A

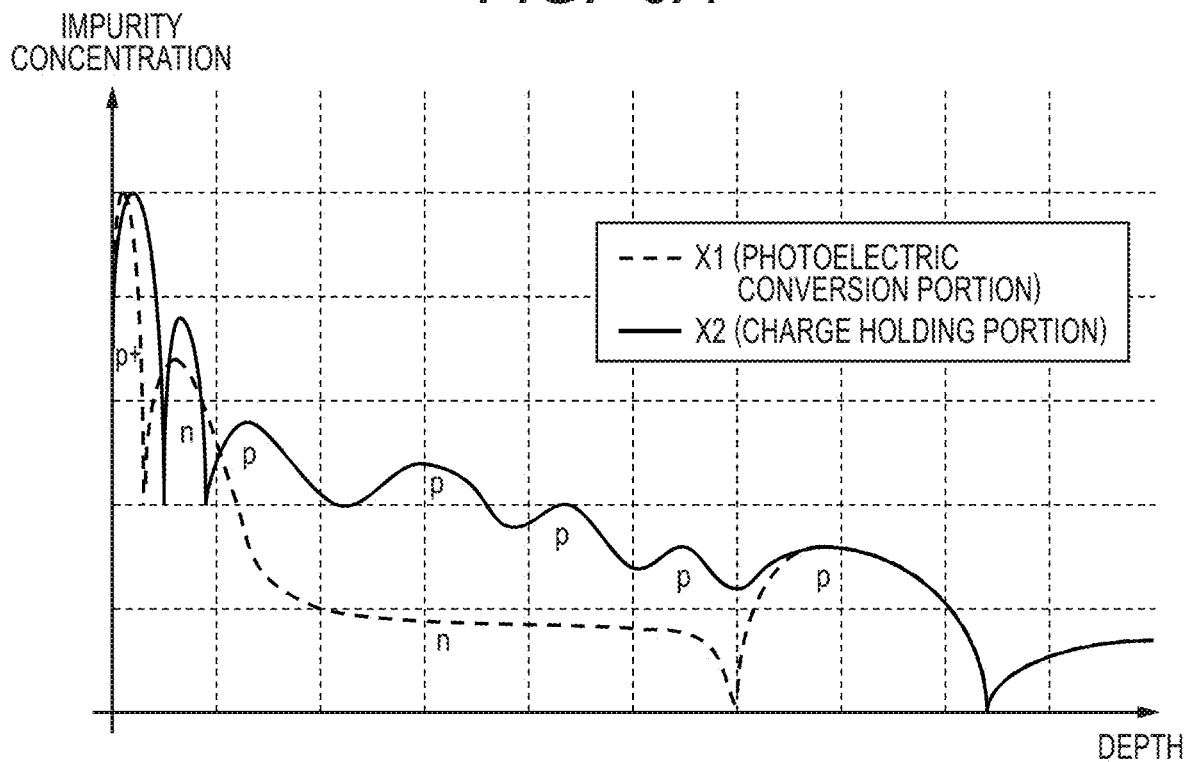
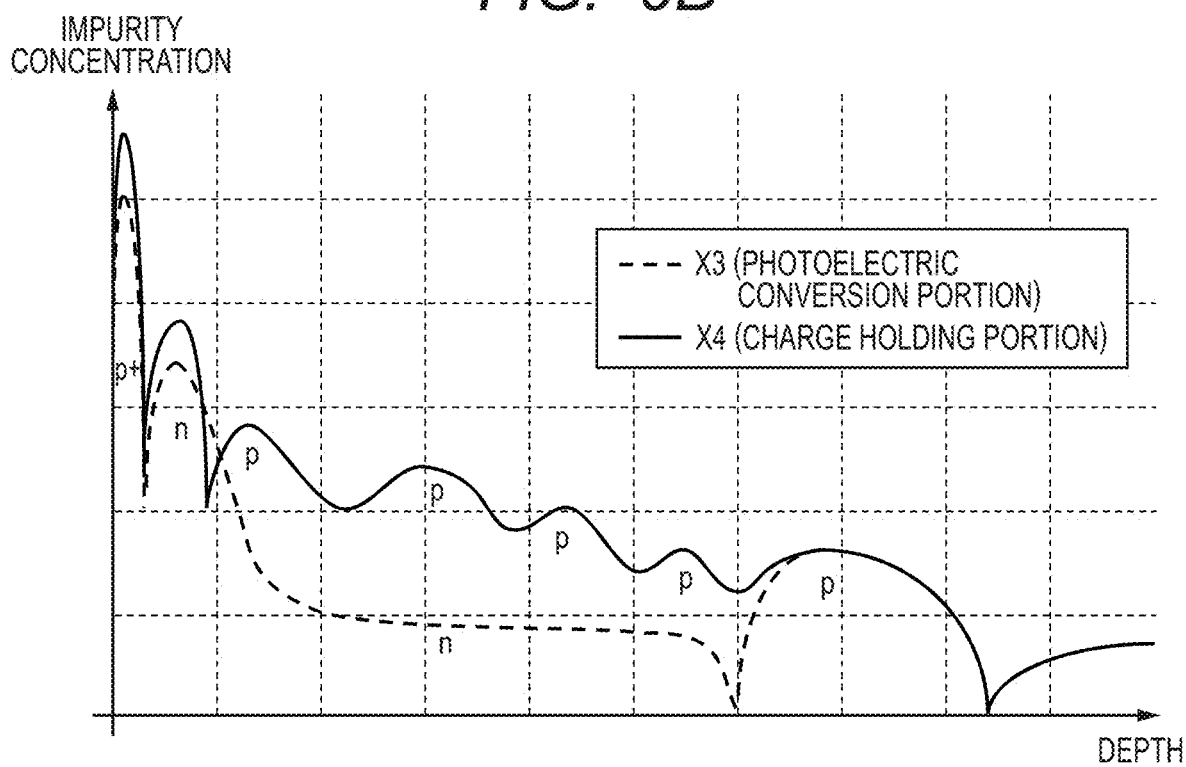


FIG. 9B



This diagram is a cross-sectional view of a semiconductor device. It shows a substrate with multiple layers labeled 7, 9, and 5. A stack of four regions, labeled 8a, 8b, 8c, and 8d, is shown on the left side. The device includes two transistors, TX1 and TX2, which are formed on the substrate. Various conductive and insulating layers are present, including layers 10, 11, 12, 31, 33, 32, 23, 24, 41, 42, 25, and 6. The device is divided into two sections, A and A', by a vertical line. The layers are labeled with 'n' and 'p' to indicate their semiconductor type. The regions 8a, 8b, 8c, and 8d are labeled with 'p' and 'p+' to indicate their semiconductor type. The regions 7, 9, and 5 are labeled with 'p' and 'n' to indicate their semiconductor type. The regions 10, 11, 12, 31, 33, 32, 23, 24, 41, 42, 25, and 6 are labeled with 'n' and 'p' to indicate their semiconductor type. The regions 10, 11, 12, 31, 33, 32, 23, 24, 41, 42, 25, and 6 are labeled with 'n' and 'p' to indicate their semiconductor type.

This cross-sectional view illustrates a semiconductor device. The substrate consists of a p-type layer (7) on top of an n-type layer (9). A stack of four p-type layers (8a, 8b, 8c, 8d) is positioned above the p-type layer (7). A gate stack (1) is located above the first transistor (TX1), comprising layers 31, 33, 32, and 23. The gate stack (1) is connected to a contact (12) on the right. The device includes two transistors, TX1 and TX2, which are formed in the substrate. TX1 has a p+ region (24) and a p+ region (41). TX2 has a p+ region (25) and a p+ region (42). A p++ region (p++) is located between the two transistors. A cross-section A-A' is indicated on the right side of the device.

FIG. 11A

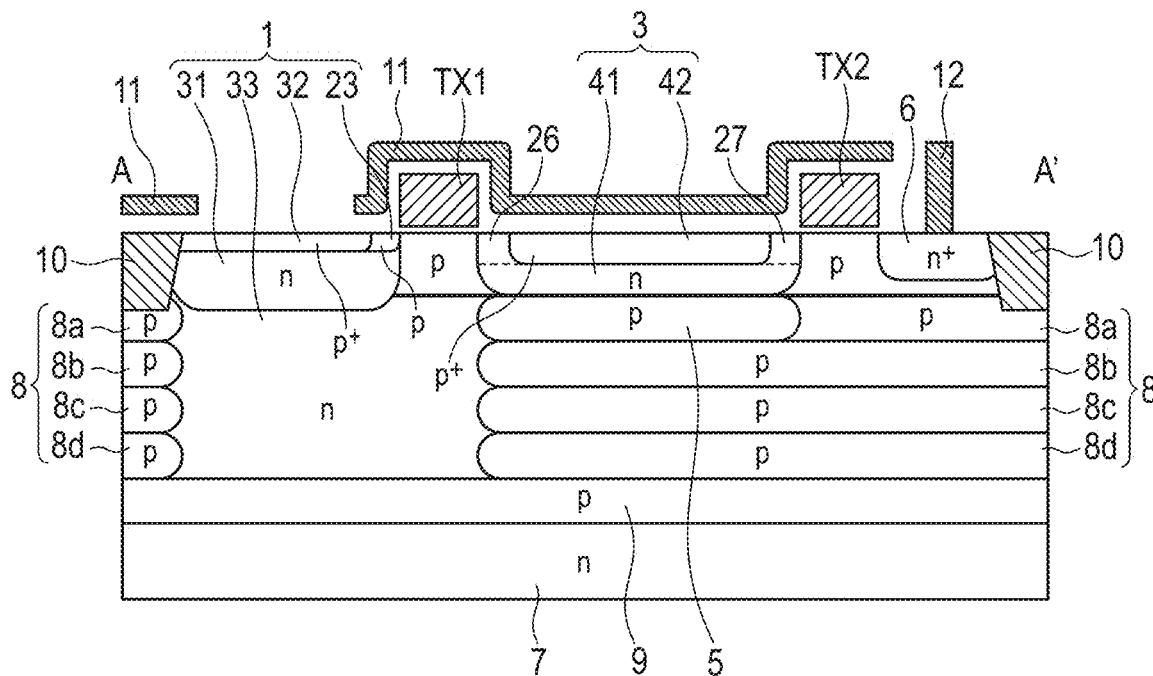


FIG. 11B

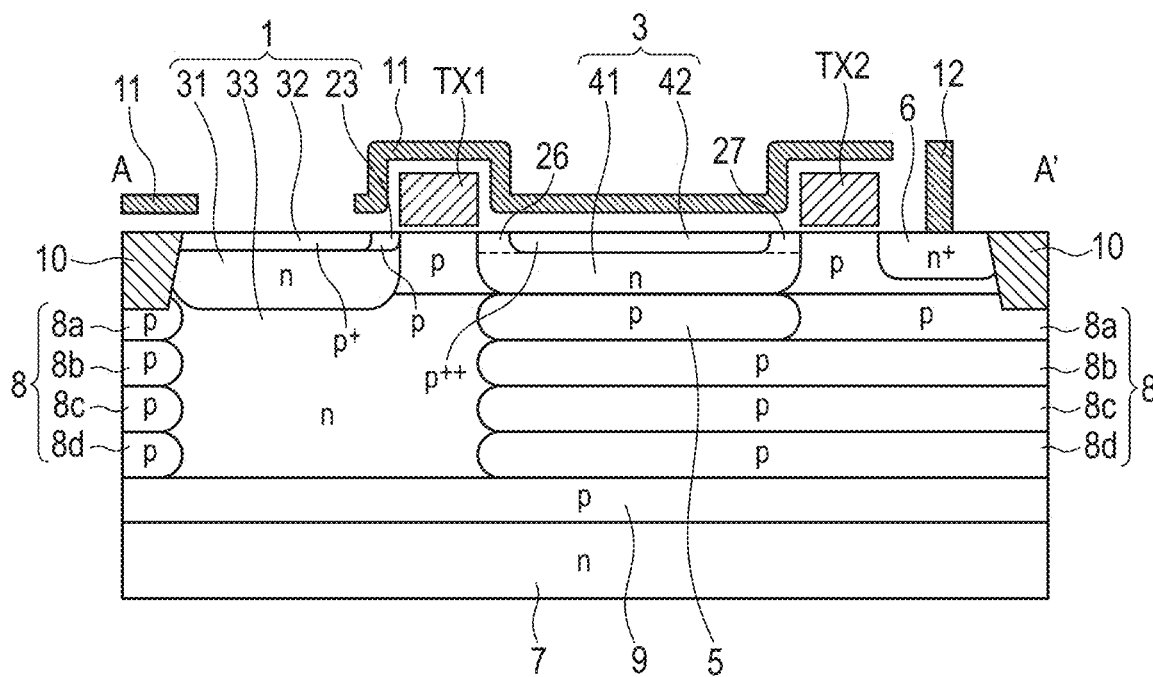


FIG. 12A

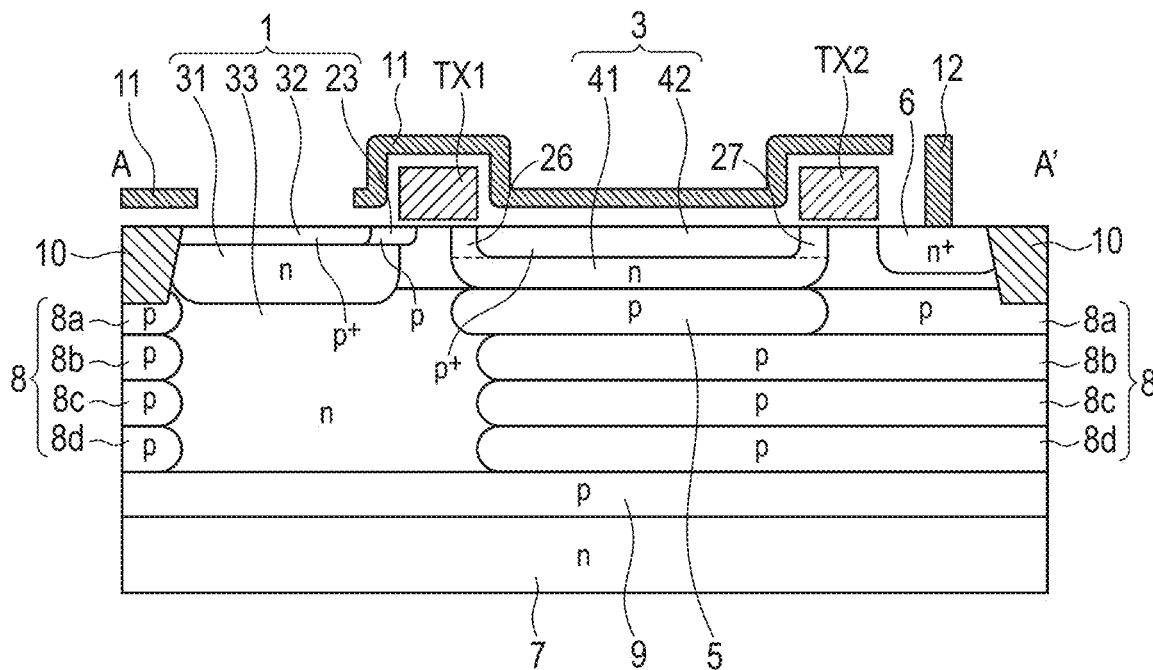


FIG. 12B

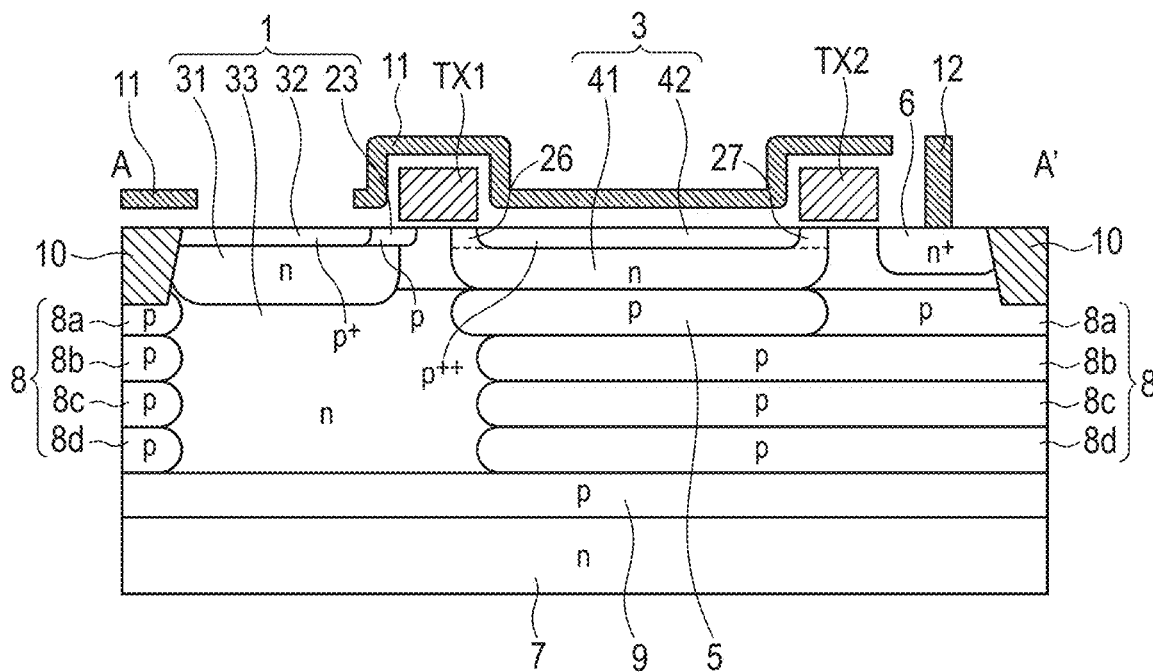
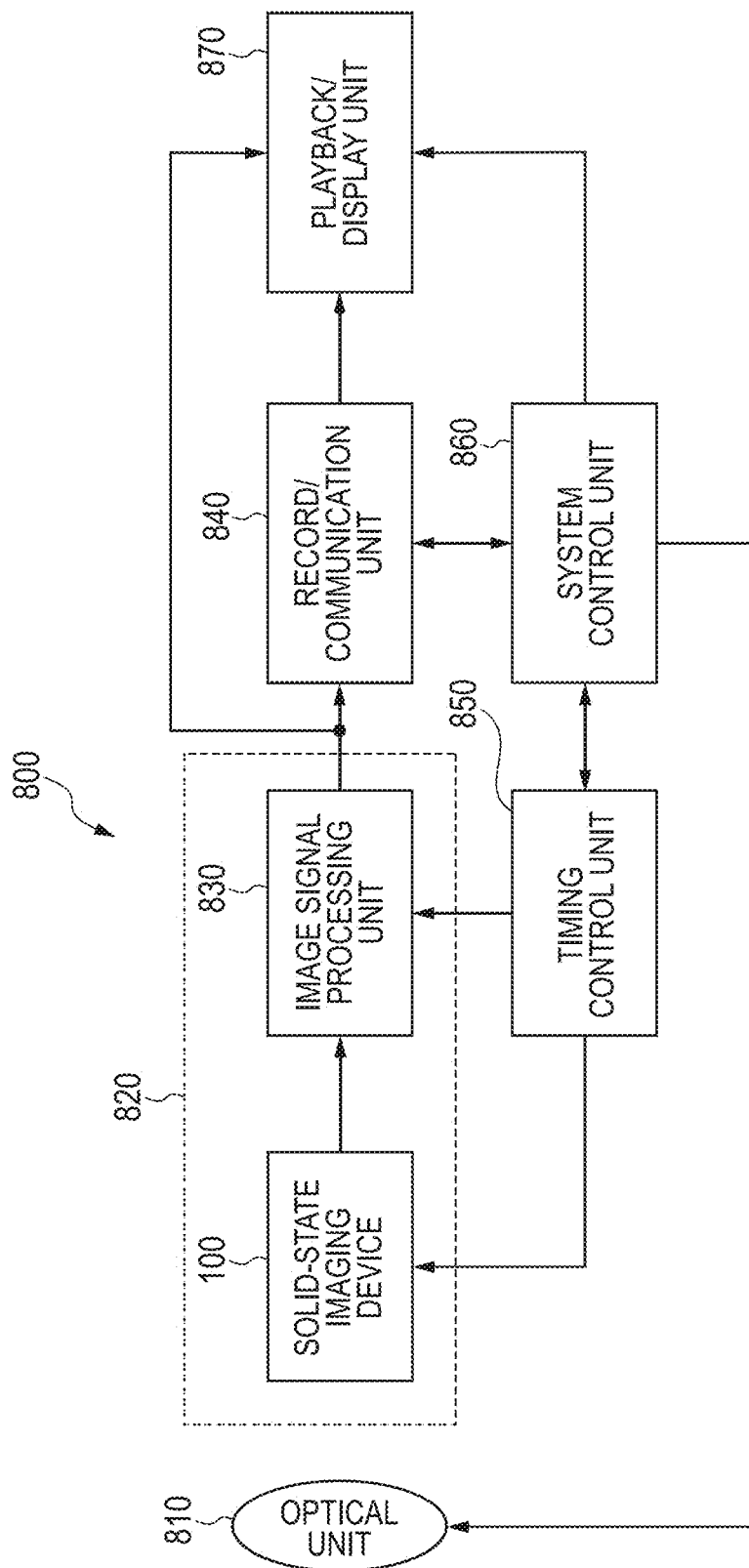


FIG. 13



SOLID-STATE IMAGING DEVICE AND IMAGING SYSTEM

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a solid-state imaging device and an imaging system.

Description of the Related Art

[0002] In recent years, an imaging system such as a digital video camera and a digital camera becomes widespread commonly, which uses a CMOS image sensor therein that is suitable for low power consumption and high-speed readout. In the CMOS image sensor, a sequentially reading out operation (rolling shutter operation) is basic which sequentially reads out pixels in every one row or in every block of several rows, but a CMOS image sensor having a function of a whole-pixel simultaneous electronic shutter is also proposed (refer to International Publication No. WO 11/043432)). Here, the whole-pixel simultaneous electronic shutter is a mechanism of simultaneously controlling the start and end of exposure with light in all of the pixels.

[0003] When the area of a charge holding portion is widened or the impurity concentration of the charge holding portion is increased so as to ensure a sufficient amount of saturation electric charges, in the CMOS image sensor, there has been the case where a dark current noise increases which is generated in the charge holding portion and an image quality lowers. In particular, when the whole-pixel simultaneous electronic shutter operates, time periods during which the charge holding portions of the pixels hold signal charges result in being different from each other. Because of this, when the dark current noise is large which is generated in the charge holding portion, the amount of the noise results in being different depending on the positions in the image, and there has been a possibility that a remarkable noise such as shading occurs. In addition, even in the case where the whole-pixel simultaneous electronic shutter is not operated, it is desired that the dark current noise is reduced which is generated in the charge holding portion.

SUMMARY OF THE INVENTION

[0004] An object of the present invention is to provide a solid-state imaging device that can reduce a dark current noise which is generated in a charge holding portion that accumulates a signal charge therein.

[0005] According to one aspect of the present invention, there is provided a solid-state imaging device including a plurality of pixels each of which includes a photoelectric conversion portion which photoelectrically converts incident light to generate a signal charge; a charge holding portion that accumulates the signal charge transferred from the photoelectric conversion portion; and a floating diffusion region to which the signal charge of the charge holding portion is transferred, wherein the photoelectric conversion portion includes a first semiconductor region of a first conductivity type, and a second semiconductor region of a second conductivity type formed under the first semiconductor region, the charge holding portion includes a third semiconductor region of the first conductivity type, and a fourth semiconductor region of the second conductivity type formed under the third semiconductor region, and a p-n

junction between the third semiconductor region and the fourth semiconductor region is positioned deeper than a p-n junction between the first semiconductor region and the second semiconductor region.

[0006] According to another aspect of the present invention, there is provided a solid-state imaging device including a plurality of pixels each of which includes a photoelectric conversion portion which photoelectrically converts incident light to generate a signal charge; a charge holding portion that accumulates the signal charge transferred from the photoelectric conversion portion; and a floating diffusion region to which the signal charge of the charge holding portion is transferred, wherein the photoelectric conversion portion includes a first semiconductor region of a first conductivity type, and a second semiconductor region of a second conductivity type formed under the first semiconductor region, the charge holding portion includes a third semiconductor region of the first conductivity type, and a fourth semiconductor region of the second conductivity type formed under the third semiconductor region, and the third semiconductor region has a higher impurity concentration than the first semiconductor region.

[0007] Further features of the present invention will become apparent from the following description of exemplary embodiments with reference to the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. 1 is a circuit diagram illustrating a configuration of an imaging region of a solid-state imaging device according to a first embodiment of the present invention.

[0009] FIG. 2 is a plan view schematically illustrating the structure of the imaging region of the solid-state imaging device according to the first embodiment of the present invention.

[0010] FIG. 3 is a schematic cross-sectional view illustrating the structure of the imaging region of the solid-state imaging device according to the first embodiment of the present invention.

[0011] FIG. 4 is a view illustrating distributions of impurity concentration in a photoelectric conversion portion and a charge holding portion in a unit pixel of the solid-state imaging device according to the first embodiment of the present invention.

[0012] FIG. 5 is a plan view schematically illustrating a structure of an imaging region of a solid-state imaging device according to a second embodiment of the present invention.

[0013] FIG. 6 is a schematic cross-sectional view illustrating the structure of the imaging region of the solid-state imaging device according to the second embodiment of the present invention.

[0014] FIG. 7 is a schematic cross-sectional view illustrating a structure of an imaging region of a solid-state imaging device according to a third embodiment of the present invention.

[0015] FIG. 8 is a view illustrating distributions of impurity concentration in a photoelectric conversion portion and a charge holding portion in a unit pixel of the solid-state imaging device according to the third embodiment of the present invention.

[0016] FIG. 9A and FIG. 9B are views illustrating distributions of impurity concentration in each of photoelectric conversion portions and charge holding portions in a unit

pixels of solid-state imaging devices according to a fourth embodiment of the present invention.

[0017] FIG. 10A and FIG. 10B are schematic cross-sectional views illustrating structures of imaging regions of solid-state imaging devices according to a fifth embodiment of the present invention.

[0018] FIG. 11A and FIG. 11B are schematic cross-sectional views illustrating structures of imaging regions of solid-state imaging devices according to a sixth embodiment of the present invention.

[0019] FIG. 12A and FIG. 12B are schematic cross-sectional views illustrating structures of imaging regions of solid-state imaging devices according to a seventh embodiment of the present invention.

[0020] FIG. 13 is a schematic view illustrating a configuration of an imaging system according to an eighth embodiment of the present invention.

DESCRIPTION OF THE EMBODIMENTS

[0021] Preferred embodiments of the present invention will now be described in detail in accordance with the accompanying drawings.

First Embodiment

[0022] A solid-state imaging device according to a first embodiment of the present invention will be described below with reference to FIG. 1 to FIG. 4.

[0023] FIG. 1 is a circuit diagram illustrating a configuration of an imaging region of a solid-state imaging device according to the present embodiment. FIG. 2 is a plan view illustrating a structure of the imaging region of the solid-state imaging device according to the present embodiment. FIG. 3 is a schematic cross-sectional view illustrating the structure of the imaging region of the solid-state imaging device according to the present embodiment. FIG. 4 is a view illustrating distributions of impurity concentration in a depth direction, in a photoelectric conversion portion and a charge holding portion in a unit pixel of the solid-state imaging device according to the present embodiment.

[0024] Firstly, the structure of the imaging region of the solid-state imaging device according to the present embodiment will be described below with reference to FIG. 1 to FIG. 4.

[0025] The imaging region of the solid-state imaging device 100 according to the present embodiment has a pixel array in which a plurality of unit pixels P1 are arranged in a two-dimensional matrix form along the row direction and the column direction, as is illustrated in FIG. 1. FIG. 1 illustrates the pixel array of three rows and three columns for the simplification of the drawing, but the number of the pixels P1 which are arranged in the row direction and the column direction is not limited in particular. Incidentally, in the present specification, the row direction shall mean a lateral direction in the drawing, and the column direction shall mean a longitudinal direction in the drawing.

[0026] The unit pixels P1 each have a photoelectric conversion portion 1, a first transfer transistor 14, a second transfer transistor 15, a reset transistor 16, a source follower transistor 17, a row select transistor 18 and an overflow transistor 19.

[0027] The anode of a photodiode which constitutes the photoelectric conversion portion 1 is connected to a ground voltage line 21, and the cathode thereof is connected to both

the source of the first transfer transistor 14 and the source of the overflow transistor 19. The drain of the first transfer transistor 14 is connected to the source of the second transfer transistor 15. The drain of the second transfer transistor 15 is connected to both the source of the reset transistor 16 and the gate of the source follower transistor 17. The drain of the reset transistor 16, the drain of the source follower transistor 17 and the drain of the overflow transistor 19 are connected to a power supply voltage line 20. The source of the source follower transistor 17 is connected to the drain of the row select transistor 18.

[0028] A connection node between the drain of the first transfer transistor 14 and the source of the second transfer transistor 15 constitutes a charge holding portion 3. In FIG. 1, the charge holding portion 3 is expressed by a capacitor which is connected between the ground voltage line 21 and the connection node between the drain of the first transfer transistor 14 and the source of the second transfer transistor 15.

[0029] A connection node among the drain of the second transfer transistor 15, the source of the reset transistor 16, and the gate of the source follower transistor 17 includes a floating diffusion region (hereinafter referred to as "FD region") 6. In FIG. 1, the FD region 6 is expressed by a capacitor which is connected between the ground voltage line 21 and the connection node among the drain of the second transfer transistor 15, the source of the reset transistor 16, and the gate of the source follower transistor 17.

[0030] For information, there is the case where the names of the source and the drain of the transistor vary depending on the conductivity type of the transistor, the function that receives attention, or the like, and there is also the case where the names are referred to as names opposite to the above described source and drain.

[0031] In each row of the pixel arrays, a signal line pTX1, a signal line pTX2, a signal line pRES, a signal line pSEL and a signal line pOFG are each arranged so as to extend in the row direction. The signal line pTX1 is connected to the gates of the first transfer transistors 14 in the unit pixels P1 which are aligned in the row direction, respectively, and forms a common signal line to these unit pixels P1. The signal line pTX2 is connected to the gates of the second transfer transistors 15 in the unit pixels P1 which are aligned in the row direction, respectively, and forms a common signal line to these unit pixels P1. The signal line pRES is connected to the gates of the reset transistors 16 in the unit pixels P1 which are aligned in the row direction, respectively, and forms a common signal line to these unit pixels P1. The signal line pSEL is connected to the gates of the row select transistors 18 in the unit pixels P1 which are aligned in the row direction, respectively, and forms a common signal line to these unit pixels P1. The signal line pOFG is connected to the gates of the overflow transistors 19 in the unit pixels P1 which are aligned in the row direction, respectively, and forms a common signal line to these unit pixels P1. Incidentally, in FIG. 1, a number corresponding to a row number n is added to each of the names of the signal lines (for instance, pTX1(n-1), pTX1(n) and pTX1(n+1)).

[0032] In each column of the pixel array, a vertical signal line Vout is arranged so as to extend in the column direction. The vertical signal line Vout is connected to the sources (pixel output portion 22) of the row select transistors 18 in the unit pixels P1 which are aligned in the column direction, respectively, and forms a common signal line to these unit

pixels P1. In FIG. 1, a number corresponding to a column number m is added to each of the names of the vertical signal lines Vout (for instance, Vout($m-1$), Vout(m) and Vout($m+1$)).

[0033] For information, the row select transistor 18 in the unit pixel P1 may be omitted. In this case, the source of the source follower transistor 17, which functions as the pixel output portion 22, is connected to the vertical signal line Vout.

[0034] The pixel array of the circuit configuration illustrated in FIG. 1 can be achieved, for instance, by a planar layout illustrated in FIG. 2. A region (hereinafter referred to as “unit pixel region”) which is surrounded by the dotted line in FIG. 2 corresponds to the unit pixel P1. This unit pixel region is repeatedly arranged in the row direction and the column direction, and thereby the pixel array is formed which is an imaging region.

[0035] In each of the unit pixel regions, an approximately inverted S-shaped active region 10a is defined by an element isolation region 10. Above the active region 10a, gate electrodes of the respective transistors are arranged. Specifically, gate electrodes TX1, TX2, RES, SFG and SEL are arranged in this order from the lower side of the active region 10a in FIG. 2 so as to traverse the active region 10a. Here, the gate electrode TX1 is the gate electrode of the first transfer transistor 14. The gate electrode TX2 is the gate electrode of the second transfer transistor 15. The gate electrode RES is the gate electrode of the reset transistor 16. The gate electrode SFG is the gate electrode of the source follower transistor 17. The gate electrode SEL is the gate electrode of the row select transistor 18.

[0036] In FIG. 2, the photoelectric conversion portion 1 is arranged in the active region 10a in the lower side of the gate electrode TX1. The charge holding portion 3 is arranged in the active region 10a between the gate electrode TX1 and the gate electrode TX2. The FD region 6 is arranged in the active region 10a between the gate electrode TX2 and the gate electrode RES. The active regions 10a of the unit pixels P1 which are adjacent to each other in the row direction are connected in a boundary between the photoelectric conversion portion 1 and the connection portion (drain region of reset transistor 16) to the power supply voltage line 20, and a gate electrode OFG of the overflow transistor 19 is arranged above this connection portion. A light-shielding layer 11 is formed above the charge holding portion 3.

[0037] Next, a structure of a portion between the photoelectric conversion portion 1 and the FD region 6 of the solid-state imaging device according to the present embodiment will be described in more detail below with reference to FIG. 3 and FIG. 4. FIG. 3 is a schematic cross-sectional view taken along the line A-A' in FIG. 2. FIG. 4 is a graph which illustrates a distribution of impurity concentration in a depth direction in a portion (photoelectric conversion portion) taken along the X1 line in FIG. 3, and a distribution of impurity concentration in a depth direction in a portion (charge holding portion) taken along the X2 line in FIG. 3. In FIG. 4, a vertical axis represents the impurity concentration (effective carrier concentration) in a form of a logarithmic axis, and both of p-type and n-type impurities are shown in a positive direction. Incidentally, here, an example of the case will be described below where an electron forms a signal charge, but a hole may form the signal charge. In this case, the conductivity type in each of the portions becomes an opposite conductivity type, correspondingly.

[0038] The photoelectric conversion portion 1 has a p-type semiconductor region 32 which is formed in the surface portion of a substrate, and an n-type semiconductor region 31 which is formed so as to come in contact with the bottom of the p-type semiconductor region 32, and forms a p-n junction between the n-type semiconductor region 31 and the p-type semiconductor region 32. The photoelectric conversion portion 1 is formed of a buried diode in which the p-n junction between the n-type semiconductor region 31 and the p-type semiconductor region 32 is formed so as to be separated from the surface of the substrate. The buried diode has an effect of being capable of reducing a noise such as a dark current which is generated at the surface of the substrate, because the p-n junction is separated from the surface of the substrate. When minority carriers which have been generated at the surface of the substrate have reached a depletion layer before being recombined, the minority carriers drift toward the n-type semiconductor region 31 of the photoelectric conversion portion 1 due to an electric field in the depletion layer. The minority carriers become easily recombined before reaching the depletion layer, because the p-n junction is separated from the surface of the substrate, which consequently can reduce the noise. Incidentally, it is desirable that the area of the charge holding portion 3 is larger than the area of the photoelectric conversion portion 1, from the viewpoint of enabling all electric charges which have been photoelectrically converted in the photoelectric conversion portion 1 to be transferred to the charge holding portion 3, while ensuring an amount of saturation electric charges. The area in the present specification is an area when the solid-state imaging device is viewed as the plane.

[0039] The photoelectric conversion portion 1 further has an n-type semiconductor region 33 which is formed so as to come in contact with the bottom of the n-type semiconductor region 31, and has a lower impurity concentration than the n-type semiconductor region 31 (see FIG. 4). The n-type semiconductor region 33 having the lower impurity concentration is arranged in a deeper portion than the n-type semiconductor region 31, and thereby the n-type semiconductor region 31 can collect even electrons which have been photoelectrically converted in a deep position that is distant from the surface of the substrate. For information, the n-type semiconductor region 33 does not necessarily need to be provided. In place of the n-type semiconductor region 33, a p-type semiconductor region may be provided in a deeper portion than the n-type semiconductor region 31. In this case, the electrons which have been photoelectrically converted in a deep position that is distant from the surface of the substrate can be collected by a depletion layer which extends to the p-type semiconductor region that has been provided in place of the n-type semiconductor region, or by a potential distribution in the p-type semiconductor region.

[0040] A p-type buried layer 9 is formed in a deeper portion than the photoelectric conversion portion 1. Thereby, the photoelectric conversion portion 1 is electrically isolated from the n-type semiconductor substrate 7 by a p-type well 8, the buried layer 9, and the like (p-n junction isolation). The buried layer 9 functions as a potential barrier between the photoelectric conversion portion 1 and the n-type semiconductor substrate 7, and has an effect of preventing the photoelectric conversion portion 1 from being mixed with unnecessary electric charges coming from the semiconductor substrate 7, and the like. Incidentally, to be exact, all of the semiconductor regions except for the gate electrode is

formed in the semiconductor substrate, but here, a portion deeper than the buried layer 9 out of the semiconductor substrate is referred to as “semiconductor substrate 7”, for the sake of convenience. The term simply expressed as “substrate” shall mean the whole of the semiconductor substrate.

[0041] The charge holding portion 3 has an n-type semiconductor region 41, and a p-type semiconductor region which is arranged in the surface side of the n-type semiconductor region 41 in terms of the substrate and forms a p-n junction between the p-type semiconductor region 42 and the n-type semiconductor region 41. The charge holding portion 3 is formed of a buried diode which reduces a noise occurring at the surface of the substrate, as in the photoelectric conversion portion 1 which has been previously described.

[0042] A p-type depletion suppression portion 5 is formed under the bottom of the charge holding portion 3 so as to come in contact with the n-type semiconductor region 41. The configuration in which the p-n junction is formed by the n-type semiconductor region 41 and the depletion suppression portion 5 has an effect of being capable of making the n-type semiconductor region 41 a completely depleted state and reading out signal charges, at low voltage. As the depletion suppression portion 5 has higher impurity concentration, the signal charges can be transferred at a lower voltage. In addition, the depletion suppression portion 5 also has an effect of preventing the charge holding portion 3 from being mixed with unnecessary electric charges which exist in deeper places than the depletion suppression portion 5.

[0043] The charge holding portion 3 and the depletion suppression portion 5 are formed in the p-type well 8. The well 8 existing in the lower part of the depletion suppression portion 5 is formed of layers formed by plural ion implantation steps, and is formed of a p-type semiconductor region which has lower impurity concentration than that of the depletion suppression portion 5 (see FIG. 4). The impurity concentration of the well 8 in the lower part of the depletion suppression portion 5 is configured to be lower than that of the depletion suppression portion 5, and thereby the charge holding portion 3 can be effectively prevented from being mixed with unnecessary electric charges. Incidentally, in FIG. 3, the well 8 is expressed by a plurality of layers 8a, 8b, 8c and 8d in order to visually illustrate that the well 8 is formed of the layers by a plurality of ion implantation steps, but functionally forms one p-type semiconductor region as a whole. The p-type buried layer 9 can also be considered as a part of the well 8. The well 8 does not necessarily need to be formed by a plurality of ion implantation steps, and the number of steps of ion implantation, which is performed so as to form the well 8, is not also limited to the illustrated example.

[0044] The light-shielding layer 11 which covers the upper part of the charge holding portion 3 is formed above the charge holding portion 3. The light-shielding layer 11 has an effect of shielding the charge holding portion 3 from incident light, and preventing the generation of unnecessary electric charges other than signal charges which are generated by photoelectric conversion in the photoelectric conversion portion 1. The light-shielding layer 11 generally employs a metal film such as tungsten and aluminum, which has a light-shielding effect against visible light, but is not limited to the above described material.

[0045] A gate electrode TX1 is formed above the semiconductor substrate between the photoelectric conversion portion 1 and the charge holding portion 3. Thereby, the first transfer transistor 14 is formed in which the n-type semiconductor region 31 functions as a source region and the n-type semiconductor region 41 functions as a drain region.

[0046] In addition, a gate electrode TX2 is formed above the semiconductor substrate between the charge holding portion 3 and the FD region 6. Thereby, the second transfer transistor 15 is formed in which the n-type semiconductor region 41 functions as a source region and the FD region 6 functions as a drain region. The FD region 6 is an n-type semiconductor region. The capacitance of the FD region 6 includes a capacitance of a p-n junction between the p-type well 8 and the n-type FD region 6. A contact plug 12 which is formed on the FD region 6 is a part of an interconnection that electrically connects the FD region 6 with the gate electrode SFG of the source follower transistor 17. Incidentally, the connection node including the FD region 6 may include a parasitic capacitance component due to these interconnections and the contact plug 12.

[0047] Next, an operation of the solid-state imaging device according to the present embodiment will be described below with reference to FIG. 1 and FIG. 3.

[0048] When light is incident on the photoelectric conversion portion 1, electrons are generated by photoelectric conversion by a photodiode of the photoelectric conversion portion 1, and these electrons are accumulated in the photoelectric conversion portion 1. When the first transfer transistor 14 is driven (turned on), the electrons which have been accumulated in the photoelectric conversion portion 1 are transferred to the charge holding portion 3.

[0049] When reading out the signal charges from pixels in a plurality of rows, a CMOS image sensor which does not have the charge holding portion sequentially drives the transfer transistors in each row (drives row by row). On the other hand, the solid-state imaging device having the charge holding portion 3 according to the present embodiment can perform the operation of simultaneously transferring the signal charges in the photoelectric conversion portions 1 in the unit pixels P1 in all of the rows to the respective charge holding portions 3, which is a whole-pixel simultaneous transfer in other words. After the whole-pixel simultaneous transfer, the photoelectric conversion portion 1 becomes a vacant state, in other words, an initial state, and becomes a start state for next exposure with light. Specifically, the solid-state imaging device according to the present embodiment can perform an operation of simultaneously controlling the start and end of exposure with light in all of the pixels, which is an operation of a whole-pixel simultaneous electronic shutter in other words.

[0050] After the signal charge has been transferred to the charge holding portion 3 from the photoelectric conversion portion 1, the overflow transistor 19 is driven so as to discharge redundant electric charges from the photoelectric conversion portion 1.

[0051] When the second transfer transistor 15 is driven (turned on), the signal charge is read out from the charge holding portion 3 to the FD region 6. When the signal charge is read out from the charge holding portion 3 to the FD region 6, the second transfer transistors 15 in each of the rows are sequentially driven (driven row by row).

[0052] When the signal charge has been read out to the FD region 6, the signal charge which has been read out to the FD

region 6 is converted into a voltage by the capacitor of the FD region 6 according to the amount of the signal charges, and the voltage is applied to the gate electrode SFG of the source follower transistor 17. The voltage which has been amplified according to the gate voltage that has been applied to the source follower transistor 17 is output to the vertical signal line Vout through the row select transistor 18. Thus, the second transfer transistors 15 in each of the rows are sequentially driven, and thereby the output signals sent from all of the pixels can be read out.

[0053] Here, because the signal is read out from the charge holding portion 3 to the FD region 6 row by row as has been described above, the time period during which the signal charge is held in the charge holding portion 3 varies depending on the position (row) of the unit pixel P1 in the screen, in other words, in the pixel array. Specifically, in a row in which a holding time period necessary for the signal charge to be transferred from the charge holding portion 3 to the FD region 6 is long, the signal charge results in being more largely affected by a dark current noise which is generated at the surface of the substrate of the charge holding portion 3, and the like. Furthermore, when the area of the charge holding portion 3 has been increased so as to ensure the saturation electric charge, the surface area of the interface increases, and accordingly the influence of the noise further increases. Incidentally, in a process of transferring the signal charge from the photoelectric conversion portion 1 to the charge holding portion 3, all of the pixels are simultaneously controlled, and accordingly the influences of the noise are not different in the screen.

[0054] For this reason, in the solid-state imaging device according to the present embodiment, in order to reduce the above described influence of the noise in the screen, the p-type semiconductor region 42 of the charge holding portion 3 is formed so as to be thicker and deeper than the p-type semiconductor region 32 of the photoelectric conversion portion 1, as is illustrated in FIG. 3 and FIG. 4. Thereby, a depletion layer region which is formed in the p-n junction between the n-type semiconductor region 41 and the p-type semiconductor region 42 of the charge holding portion 3 becomes away from the surface of the substrate, and the influence of the dark current noise can be reduced.

[0055] Incidentally, when the p-type semiconductor region 32 of the photoelectric conversion portion 1 is thickened, the p-n junction surface of the photoelectric conversion portion 1 becomes away from the surface of the substrate, and a photoelectric conversion efficiency of the incident light having a short wavelength decreases. Then, there is a concern that the gradation of a color component having a short wavelength such as blue, for instance, results in being lowered. Because of this, it is not necessarily desirable to thicken both the p-type semiconductor region 32 of the photoelectric conversion portion 1 and the p-type semiconductor region 42 of the charge holding portion 3. From such a viewpoint, it is desirable to form the p-type semiconductor region 42 of the charge holding portion 3 so as to be thicker and deeper than the p-type semiconductor region 32 of the photoelectric conversion portion 1, regardless of the p-type semiconductor region 32 of the photoelectric conversion portion 1.

[0056] Methods for forming the p-type semiconductor region 42 of the charge holding portion 3 so as to be deeper than the p-type semiconductor region 32 of the photoelectric conversion portion 1 include a method of appropriately

changing ion implantation conditions, as one example. For instance, an acceleration voltage for the ion implantation of a p-type impurity, which is set when the p-type semiconductor region 32 is formed, is set at a higher voltage than an accelerating voltage for the ion implantation of a p-type impurity, which is set when the p-type semiconductor region 42 is formed, and thereby the p-type semiconductor region 32 can be formed into a deeper place. Alternatively, it is also possible to set the acceleration voltage for the ion implantation of an n-type impurity, which is set when the n-type semiconductor region is formed, at a higher voltage than the accelerating voltage for the ion implantation of an n-type impurity, which is set when the n-type semiconductor region 31 is formed, and to form the p-n junction of the charge holding portion 3 so as to be deeper than the p-n junction of the photoelectric conversion portion 1. For information, the forming method is not limited to the above described methods, and can be appropriately changed in the range in which the present embodiment can be applied.

[0057] Thus, according to the present embodiment, the p-n junction of the charge holding portion is formed so as to be deeper than the p-n junction of the photoelectric conversion portion, and accordingly a dark current noise which is generated in the charge holding portion is reduced, and a noise component which is superimposed on a signal output from a pixel can be reduced. In addition, when the whole-pixel simultaneous electronic shutter is operated, a difference of the amount of the noise among the positions in the pixels can be reduced. Thereby, a solid-state imaging device can be achieved which has high performance and can obtain the image information of high quality.

Second Embodiment

[0058] A solid-state imaging device according to a second embodiment of the present invention will be described below with reference to FIG. 5 and FIG. 6. Similar components to those in the solid-state imaging device according to the first embodiment illustrated in FIG. 1 to FIG. 4 are designated by the same reference numerals, and the description will be omitted or simplified.

[0059] FIG. 5 is a plan view illustrating a structure of a solid-state imaging device according to the present embodiment. FIG. 6 is a schematic cross-sectional view illustrating the structure of the solid-state imaging device according to the present embodiment. Incidentally, FIG. 6 is a cross-sectional view taken along the line C-C' in FIG. 5.

[0060] The solid-state imaging device according to the present embodiment is similar to the solid-state imaging device according to the first embodiment, except that the pattern of the gate electrode TX1 of the first transfer transistor 14 is different from that in the first embodiment, as is illustrated in FIG. 5 and FIG. 6. Specifically, in the solid-state imaging device according to the present embodiment, the gate electrode TX1 of the first transfer transistor 14 is formed not only in the region between the photoelectric conversion portion 1 and the charge holding portion 3, but also is formed so as to extend to the upper part of the charge holding portion 3.

[0061] The gate electrode TX1 is formed into such a pattern, and thereby the potential can be lowered in the most regions of the charge holding portion 3, when an ON voltage has been applied to the gate electrode TX1 of the first transfer transistor 14, when the electric charge is transferred from the photoelectric conversion portion 1 to the charge

holding portion 3. Thereby, the electric charges can be easily transferred from the photoelectric conversion portion 1 to the charge holding portion 3.

[0062] The structure in which the electric charges are easily transferred shows also an effect of lowering the ON voltage of the first transfer transistor 14 than an ON voltage in the case where the gate electrode TX1 does not extend to the upper part of the charge holding portion 3, and being capable of reducing the electric power consumption.

[0063] In addition, when an OFF voltage is applied to the gate electrode TX1 of the first transfer transistor 14, the pinning of the surface of the substrate can be performed, which originates in that there is the p-type semiconductor region 42 of the charge holding portion 3 and besides the first transfer transistor 14 is set at the OFF voltage. Thereby, the dark current noise of the charge holding portion 3 can be further reduced.

[0064] Thus, according to the present embodiment, the gate electrode TX1 of the first transfer transistor 14 is formed so as to extend to the upper part of the charge holding portion 3. Accordingly, the electric charges can be easily transferred from the photoelectric conversion portion 1 to the charge holding portion 3, and also the dark current noise of the charge holding portion 3 can be further reduced.

Third Embodiment

[0065] A solid-state imaging device according to a third embodiment of the present invention will be described below with reference to FIG. 7 and FIG. 8. Similar components to those in the solid-state imaging devices according to the first and second embodiments illustrated in FIG. 1 to FIG. 6 are designated by the same reference numerals, and the description will be omitted or simplified.

[0066] FIG. 7 is a schematic cross-sectional view illustrating a structure of a solid-state imaging device according to the present embodiment. FIG. 8 is a view illustrating distributions of impurity concentration in a depth direction, in a photoelectric conversion portion and a charge holding portion in the solid-state imaging device according to the present embodiment. Incidentally, FIG. 7 is a cross-sectional view of a portion corresponding to the portion taken along the line A-A' in FIG. 2. In addition, FIG. 8 is a graph illustrating a distribution of impurity concentration in a depth direction, in each of a portion (photoelectric conversion portion) taken along the X3 line in FIG. 7, and a portion (charge holding portion) taken along the X4 line in FIG. 7. In FIG. 8, a vertical axis represents the impurity concentration (effective carrier concentration) in a form of a logarithmic axis, and both of p-type and n-type impurities are shown in a positive direction.

[0067] The solid-state imaging device according to the present embodiment is similar to the solid-state imaging device according to the first embodiment, except that the profile of the impurity in the p-type semiconductor region 42 of the charge holding portion 3 is different from that in the first embodiment, as is illustrated in FIG. 7 and FIG. 8. Specifically, in the solid-state imaging device according to the present embodiment, the impurity concentration of the p-type semiconductor region 42 of the charge holding portion 3 is higher than the case in the first embodiment illustrated in FIG. 4.

[0068] When the impurity concentration of the p-type semiconductor region 42 of the charge holding portion 3 is controlled so as to become high, a depletion layer region

which is generated at the p-n junction between the n-type semiconductor region 41 and the p-type semiconductor region 42 of the charge holding portion 3 becomes away from the surface of the substrate. This is because as the semiconductor region has a higher impurity concentration, the width of the depletion layer which extends from the p-n junction is smaller. As a result, the influence of the dark current noise can be reduced.

[0069] Incidentally, when the impurity concentration in the p-type semiconductor region 32 of the photoelectric conversion portion 1 has been controlled so as to become high, the depletion layer region which is generated at the p-n junction between the n-type semiconductor region 41 and the p-type semiconductor region 42 is further widened to the side of the n-type semiconductor region 41. Accordingly, there is a concern that a photoelectric conversion efficiency of incident light having a short wavelength decreases. Because of this, it is not necessarily desirable to control impurity concentrations of both the p-type semiconductor region 32 of the photoelectric conversion portion 1 and the p-type semiconductor region 42 of the charge holding portion 3 so as to become high. From such a viewpoint, it is desirable to form the p-type semiconductor region 42 of the charge holding portion 3 so as to have a higher impurity concentration than that in the p-type semiconductor region 32 of the photoelectric conversion portion 1, regardless of the p-type semiconductor region 32 of the photoelectric conversion portion 1.

[0070] Methods for forming the p-type semiconductor region 42 of the charge holding portion 3 so as to have a higher impurity concentration than that in the p-type semiconductor region 32 of the photoelectric conversion portion 1 include appropriately changing ion implantation conditions, as one example. For instance, an ion implantation step for forming the p-type semiconductor region 32 is separated from an ion implantation step for forming the p-type semiconductor region 42, and the dose in ion implantation is increased, which is set when the p-type semiconductor region 42 is formed. Thereby the impurity concentration in the p-type semiconductor region 42 can be controlled so as to become high. Alternatively, after the ions have been implanted into the photoelectric conversion portion 1 and the charge holding portion 3 on the ion implantation conditions of the p-type semiconductor region 32, ions are additionally implanted into the charge holding portion 3. Thereby the impurity concentration in the p-type semiconductor region 42 can be controlled so as to become high. For information, the forming method is not limited to the above described methods, and can be appropriately changed in the range in which the present embodiment can be applied.

[0071] Thus, according to the present embodiment, the p-type semiconductor region 42 of the charge holding portion 3 is formed so as to have the higher impurity concentration than that in the p-type semiconductor region 32 of the photoelectric conversion portion 1, and accordingly the dark current noise of the charge holding portion can be reduced.

Fourth Embodiment

[0072] A solid-state imaging device according to a fourth embodiment of the present invention will be described below with reference to FIG. 9A and FIG. 9B. Similar components to those in the solid-state imaging devices according to the first to third embodiments illustrated in FIG.

1 to FIG. 8 are designated by the same reference numerals, and the description will be omitted or simplified.

[0073] FIG. 9A and FIG. 9B are views illustrating distributions of impurity concentrations in a depth direction, in each of photoelectric conversion portions and charge holding portions of solid-state imaging devices according to the present embodiment. Incidentally, FIG. 9A is a graph illustrating distributions of impurity concentration in a depth direction, in a portion (photoelectric conversion portion) taken along the X1 line in FIG. 3, and a portion (charge holding portion) taken along the X2 line in FIG. 3. FIG. 9B is a graph illustrating distributions of impurity concentration in a depth direction, in a portion (photoelectric conversion portion) taken along the X3 line in FIG. 7, and a portion (charge holding portion) taken along the X4 line in FIG. 7.

[0074] In FIG. 9A and FIG. 9B, a vertical axis represents the impurity concentration (effective carrier concentration) in a form of a logarithmic axis, and both of p-type and n-type impurities are shown in a positive direction.

[0075] The solid-state imaging device according to the present embodiment is configured to be similar to the solid-state imaging devices according to the first to third embodiments, except that profiles of the impurity in the n-type semiconductor region 41 of the charge holding portion are different from those in the first to third embodiments. Specifically, in the solid-state imaging device according to the present embodiment, the impurity concentration in the n-type semiconductor region 41 of the charge holding portion 3 becomes higher than the impurity concentration in the n-type semiconductor region 31 of the photoelectric conversion portion 1, as is illustrated in FIG. 9A and FIG. 9B.

[0076] Here, FIG. 9A illustrates the distribution of impurity concentration in a depth direction, in each of the photoelectric conversion portion 1 and the charge holding portion 3, in the case where the configuration of the present embodiment has been applied to the solid-state imaging device of the first or second embodiment. In addition, FIG. 9B illustrates the distribution of impurity concentration in a depth direction, in each of the photoelectric conversion portion 1 and the charge holding portion 3, in the case where the configuration of the present embodiment has been applied to the solid-state imaging device of the third embodiment.

[0077] The reason will be described below why the n-type semiconductor region 41 of the charge holding portion 3 is formed so as to have a higher impurity concentration than an impurity concentration in the n-type semiconductor region 31 of the photoelectric conversion portion 1, in the solid-state imaging device according to the present embodiment.

[0078] The first reason is because the amount of electric charges which can be accumulated by the charge holding portion 3 becomes larger than the amount of electric charges which can be accumulated by the photoelectric conversion portion 1. The amount of saturation electric charges in the solid-state imaging device of the present invention is the amount of electric charges that can be accumulated by a portion in which the signal charge is accumulated when being read out row by row, specifically, by the charge holding portion 3. If the amount of electric charges which can be accumulated by the photoelectric conversion portion 1 is larger than the amount of electric charges which can be accumulated by the charge holding portion 3, all of the electric charges which have been photoelectrically con-

verted in the photoelectric conversion portion 1 cannot be transferred to the charge holding portion 3, and the amount of the saturation electric charges is limited by the amount of the electric charges which can be accumulated by the charge holding portion 3. On the contrary, if the amount of electric charges which can be accumulated by the photoelectric conversion portion 1 is smaller than the amount of electric charges which can be accumulated by the charge holding portion 3, the amount of saturation electric charges can be set so as to be the amount of electric charges which can be accumulated by the charge holding portion 3, through an operation of transferring the electric charges from the photoelectric conversion portion 1 to the charge holding portion 3 multiple times. Accordingly, in order to ensure the amount of the saturation electric charges within a limited region, the amount of the electric charges which can be accumulated by the charge holding portion 3 can be set so as to be larger than the amount of the electric charges which can be accumulated by the photoelectric conversion portion 1.

[0079] The amount of the saturation electric charges in the photoelectric conversion portion 1 can be increased more than the amount of the electric charges which can be accumulated by the charge holding portion 3, through the operation of transferring the electric charges from the charge holding portion 3 to the FD region 6 multiple times. However, in this case as well, the amount of the electric charges which can be accumulated by the charge holding portion 3 can be set so as to be larger than the amount of the electric charges which can be accumulated by the photoelectric conversion portion 1.

[0080] The second reason is because the amount of saturation electric charges in the charge holding portion 3 is ensured. In the deep portion of the charge holding portion 3, the depletion suppression portion 5 of the p-type is formed which is an opposite conductivity type, and accordingly the concentration of the n-type impurity in the n-type semiconductor region 41 which is formed on the upper part of the depletion suppression portion 5 results in being small, compared to that in the n-type semiconductor region 31. When the n-type semiconductor region 41 of the charge holding portion 3 is formed so as to have a higher impurity concentration than an impurity concentration in the n-type semiconductor region 31 of the photoelectric conversion portion 1, the decrease of the concentration of the n-type impurity in the n-type semiconductor region 41 is suppressed, and a sufficient amount of saturation electric charges can be ensured.

[0081] As has been described in the two reasons, it is appropriate to form the n-type semiconductor region 41 of the charge holding portion 3 so as to have a higher impurity concentration than an impurity concentration in the n-type semiconductor region 31 of the photoelectric conversion portion 1.

[0082] However, if the n-type semiconductor region 41 of the charge holding portion 3 is simply formed so as to have a high impurity concentration, the concentration of the p-type impurity in the p-type semiconductor region 42 of the charge holding portion 1 decreases, and the charge holding portion results in being easily affected by the dark current noise on the surface of the substrate.

[0083] For this reason, it is desirable to form the p-type semiconductor region 42 of the charge holding portion so as to be thicker and deeper than the p-type semiconductor region 32 of the photoelectric conversion portion 1, as is

illustrated in FIG. 9A. Alternatively, it is desirable to form the p-type semiconductor region 42 of the charge holding portion 3 so as to have a higher impurity concentration than that in the p-type semiconductor region 32 of the photoelectric conversion portion 1, as is illustrated in FIG. 9B. By having such a configuration, the solid-state imaging device can suppress the influence of the dark current noise in the photoelectric conversion portion 3 and increase the amount of the saturation electric charges therein, at the same time.

[0084] Thus, according to the present embodiment, the n-type semiconductor region 41 of the charge holding portion 3 is formed so as to have a higher impurity concentration than that in the n-type semiconductor region 31 of the photoelectric conversion portion 1, and accordingly the amount of the saturation electric charges can be increased.

Fifth Embodiment

[0085] A solid-state imaging device according to a fifth embodiment of the present invention will be described below with reference to FIG. 10A and FIG. 10B. Similar components to those in the solid-state imaging devices according to the first to fourth embodiments illustrated in FIG. 1 to FIG. 9B are designated by the same reference numerals, and the description will be omitted or simplified. [0086] FIG. 10A and FIG. 10B are schematic cross-sectional views illustrating the structures of the solid-state imaging devices according to the present embodiment. Incidentally, FIG. 10A and 10B are cross-sectional views of portions corresponding to the portion taken along the line A-A' in FIG. 2.

[0087] The solid-state imaging device according to the present embodiment is similar to the solid-state imaging devices according to the first to fourth embodiments, except that the structures of the p-type semiconductor region 32 of the photoelectric conversion portion 1 and the p-type semiconductor region 42 of the charge holding portion 3 are different from those in the first to fourth embodiments. Specifically, the solid-state imaging device according to the present embodiment has an electric field suppression layer 23 which has a lower impurity concentration than that of the p-type semiconductor region 32, on the end in the side of the charge holding portion, in other words, on the end in the side of the gate electrode TX1, of the p-type semiconductor region 32, as is illustrated in FIG. 10A and FIG. 10B. In addition, the solid-state imaging device has an electric field suppression layer 24 which has a lower impurity concentration than that in the p-type semiconductor region 42, on the end in the side of the photoelectric conversion portion, in other words, on the end in the side of the gate electrode TX1, of the p-type semiconductor region 42. In addition, the solid-state imaging device has an electric field alleviation layer 25 which has a lower impurity concentration than that in the p-type semiconductor region 42, on the end in the side of the FD region 6, in other words, on the end in the side of the gate electrode TX2, of the p-type semiconductor region 42. FIG. 10A is a schematic cross-sectional view in the case where the configuration of the present embodiment has been applied to the solid-state imaging devices of the first, second and fourth embodiments. In addition, FIG. 10B is a schematic cross-sectional view in the case where the configuration of the present embodiment has been applied to the solid-state imaging device of the third embodiment.

[0088] When the electric charges are transferred, an electric field is generated which is caused by a potential differ-

ence between a voltage (for instance, 3.3 V) to be applied to the gate electrodes TX1 and TX2 and a potential (for instance, 0 V) of the p-type semiconductor regions 32 and 42. There is a concern that unnecessary electric charges are generated by a phenomenon which is referred to as impact ionization that occurs due to this electric field and/or an electric field in the depletion layer region which is generated at the p-n junction in the photoelectric conversion portion 1 and the charge holding portion 3, and that the noise results in increasing.

[0089] When the electric field suppression layers 23, 24 and 25 are provided, potential gradients can be suppressed in between the gate electrode TX1 and the photoelectric conversion portion 1, in between the gate electrode TX1 and the charge holding portion 3, and in between the charge holding portion 3 and the gate electrode TX2, when the electric charges are transferred. Thereby, the electric field intensity in each of the above described portions can be weakened, and the increase of the noise can be prevented.

[0090] In addition, potential barriers are also lowered in between the photoelectric conversion portion 1 and the first transfer transistor 14, in between the first transfer transistor 14 and the charge holding portion 3, and in between the charge holding portion 3 and the second transfer transistor 15. Accordingly, an effect of facilitating the transfer of the electric charges is also obtained.

[0091] Thus, according to the present embodiment, the electric field suppression layers 23, 24 and 25 are provided on the ends of the p-type semiconductor regions 32 and 42. Accordingly, the noise is reduced which is generated when the signal charge is transferred, and the charge can be easily transferred.

Sixth Embodiment

[0092] A solid-state imaging device according to a sixth embodiment of the present invention will be described below with reference to FIG. 11A and FIG. 11B. Similar components to those in the solid-state imaging devices according to the first to fifth embodiments illustrated in FIG. 1 to FIG. 10B are designated by the same reference numerals, and the description will be omitted or simplified.

[0093] FIG. 11A and FIG. 11B are schematic cross-sectional views illustrating the structures of the solid-state imaging devices according to the present embodiment. Incidentally, FIG. 11A and FIG. 11B are cross-sectional views of portions corresponding to the portion taken along the line A-A' in FIG. 2.

[0094] The solid-state imaging device according to the present embodiment is similar to the solid-state imaging device according to the fifth embodiment, except that the structure of the n-type semiconductor region 41 of the charge holding portion 3 is different from that in the fifth embodiment. Specifically, the solid-state imaging device according to the present embodiment has a transfer support layer 26 provided in the side of the photoelectric conversion portion of the p-type semiconductor region 42, specifically, in the vicinity of the gate electrode TX1, as is illustrated in FIG. 11A and FIG. 11B. In addition, a transfer support layer 27 is provided in the side of the FD region 6 of the p-type semiconductor region 42, specifically, in the vicinity of the gate electrode TX2. The transfer support layers 26 and 27 are formed of an n-type semiconductor region which has conductivity opposite to that in the p-type semiconductor

region 42. In the examples of FIG. 11A and FIG. 11B, a part of the n-type semiconductor region 41 is the transfer support layers 26 and 27.

[0095] FIG. 11A is a schematic cross-sectional view in the case where the transfer support layers 26 and 27 are provided in the solid-state imaging device according to the fifth embodiment illustrated in FIG. 10A. In addition, FIG. 11B is a schematic cross-sectional view in the case where the auxiliary transfer layers 26 and 27 are provided in the solid-state imaging device according to the fifth embodiment illustrated in FIG. 10B. It can be also said that the solid-state imaging device according to the present embodiment has the n-type transfer support layers 26 and 27 arranged in place of the p-type electric field suppression layers 24 and 25, from a relationship between the solid-state imaging device according to the present embodiment and the solid-state imaging device according to the fifth embodiment illustrated in FIG. 10A and FIG. 10B.

[0096] When the transfer support layers 26 and 27 are provided, an effect of reducing the electric field is obtained that is generated in each of the portions when the electric charges are transferred, which is similar to the effect described in the fifth embodiment. In addition, potential barriers are lowered in between the photoelectric conversion portion 1 and the first transfer gate TX1, in between the first transfer gate TX1 and the charge holding portion 3, and in between the charge holding portion 3 and the second transfer gate TX2. Accordingly, an effect of facilitating the transfer of the electric charges is also obtained.

[0097] For information, both of the two transfer support layers 26 and 27 do not necessarily need to be provided, and only any one layer may be provided. In this case as well, a potential barrier in a portion in which the transfer support layer 26 or the transfer support layer 27 has been arranged is lowered, and accordingly an effect of facilitating the transfer of the electric charges is obtained.

[0098] The transfer support layers 26 and 27 may be simultaneously formed in a step of forming the n-type semiconductor region 41 (as a part of the n-type semiconductor region 41), or may also be formed in a step different from the step of forming the n-type semiconductor region 41.

[0099] Thus, according to the present embodiment, the transfer support layers 26 and 27 are provided on the ends of the p-type semiconductor region 42, and accordingly the electric charges can be easily transferred.

Seventh Embodiment

[0100] A solid-state imaging device according to a seventh embodiment of the present invention will be described below with reference to FIG. 12A and FIG. 12B. Similar components to those in the solid-state imaging devices according to the first to sixth embodiments illustrated in FIG. 1 to FIG. 11B are designated by the same reference numerals, and the description will be omitted or simplified.

[0101] FIG. 12A and FIG. 12B are schematic cross-sectional views illustrating the structures of the solid-state imaging devices according to the present embodiment. Incidentally, FIG. 12A and FIG. 12B are cross-sectional views of portions corresponding to the portion taken along the line A-A' in FIG. 2.

[0102] The solid-state imaging device according to the present embodiment is similar to the solid-state imaging device according to the sixth embodiment, except that the

electric field suppression layer 23 and the transfer support layers 26 and 27 extend to regions below the gate electrodes TX1 and TX2. Specifically, in the solid-state imaging device according to the present embodiment, the electric field suppression layer 23 extends to a region below the gate electrode TX1, as is illustrated in FIG. 12A and FIG. 12B. In addition, the transfer support layer 26 extends to a region below the gate electrode TX1. In addition, the transfer support layer 27 extends to a region below the gate electrode TX2. FIG. 12A is an example in which the configuration of the present embodiment has been applied to the solid-state imaging device according to the sixth embodiment illustrated in FIG. 11A, and FIG. 12B is an example in which the configuration of the present embodiment is applied to the solid-state imaging device according to the sixth embodiment illustrated in FIG. 11B.

[0103] The electric field suppression layer 23 and the transfer support layers 26 and 27 are arranged so as to extend to the lower regions of the gate electrodes TX1 and TX2, and thereby potential barriers below the gate electrodes TX1 and TX2 can be reduced. Thereby, the electric charges can be further easily transferred.

[0104] For information, all of the electric field suppression layer 23 and the transfer support layers 26 and 27 do not necessarily need to be formed so as to extend to the lower regions of the gate electrodes TX1 and TX2. It is also acceptable to form any one or two layers so as to extend to the lower regions of the gate electrodes TX1 and TX2.

[0105] Thus, according to the present embodiment, the electric field suppression layer 23 and the transfer support layers 26 and 27 are formed so as to extend to the lower regions of the gate electrodes TX1 and TX2, and accordingly the electric charges can be easily transferred.

Eighth Embodiment

[0106] An imaging system according to an eighth embodiment of the present invention will be described below with reference to FIG. 13. Similar components to those in the solid-state imaging devices according to the first to seventh embodiments illustrated in FIG. 1 to FIG. 12B are designated by the same reference numerals, and the description will be omitted or simplified.

[0107] FIG. 13 is a view illustrating a configuration example of an imaging system according to the present embodiment. An imaging system 800 includes, for instance, an optical unit 810, a solid-state imaging device 100, an image signal processing unit 830, a record/communication unit 840, a timing control unit 850, a system control unit 860, and a playback/display unit 870. The imaging device 820 has the solid-state imaging device 100 and the video signal processing unit 830. The solid-state imaging device 100 employs any of the solid-state imaging devices 100 which have been described in the previous embodiments.

[0108] The optical unit 810 that is an optical system such as a lens focuses an image of light emitted from an object onto a pixel unit of the solid-state imaging device 100, in which a plurality of unit pixels P1 are two-dimensionally arranged, and forms an image of the object (object image) on the pixel unit. The solid-state imaging device 100 outputs signals according to the light of which the image has been focused on the pixel unit, on the timing based on the signal output from the timing control unit 850. The signals output from the solid-state imaging device 100 are input into the image signal processing unit 830, and the image signal

processing unit **830** performs signal processing with a specified method by a program or the like. The signals obtained by the processing in the image signal processing unit **830** are transmitted to the record/communication unit **840** as image data. The record/communication unit **840** transmits signals for forming an image to the playback/display unit **870**, and makes the playback/display unit **870** playbacks and displays a moving image or a still image. The record/communication unit **840** also communicates with the system control unit **860** by receiving the signals transmitted from the image signal processing unit **830**, and besides, performs an operation of recording the signals for forming the image on an unillustrated recording medium.

[0109] The system control unit **860** is a unit for collectively controlling an operation of the imaging system, and controls drives of the optical unit **810**, the timing control unit **850**, the record/communication unit **840** and the playback/display unit **870**. In addition, the system control unit **860** is provided, for instance, with an unillustrated storage device that is a recording medium, and records a program and the like which are necessary for controlling the operation of the imaging system, in the storage device. The system control unit **860** also supplies, for instance, a signal which switches driving modes according to an operation of a user, into the imaging system. Specific examples include a signal for a change of a row to be read out or a row to be reset, a signal for a change of an angle of view, which accompanies an operation of an electronic zoom, and a signal for a shift of an angle of view, which accompanies electronic vibration control. The timing control unit **850** controls the driving timings for the solid-state imaging device **100** and the image signal processing unit **830** based on the control by the system control unit **860**.

[0110] Thus, the imaging system is configured to which any of the solid-state imaging devices according to the first to seventh embodiments is applied, and thereby an imaging system can be configured which uses a solid-state imaging device that has a function of a whole-pixel simultaneous electronic shutter and has high performance.

Modified Embodiment

[0111] The present invention is not limited to the above described embodiments, but can be modified in various ways.

[0112] The above described embodiments have been described assuming that the solid-state imaging device has the function of the whole-pixel simultaneous electronic shutter, for instance, but the configurations of the solid-state imaging devices described in the above described embodiments are not necessarily limited only to the solid-state imaging device which operates the whole-pixel simultaneous electronic shutter.

[0113] In addition, in the above described third embodiment, the p-type semiconductor region **42** is formed so as to have a high impurity concentration, and in the above described first and second embodiments, the p-type semiconductor region **42** is thickly formed. However, the p-type semiconductor region **42** may also be formed so as to be thick and have a high impurity concentration.

[0114] In addition, in the above described sixth embodiment, the transfer support layers **26** and **27** are provided in the vicinity of the gate electrodes TX1 and TX2 of the p-type semiconductor region **42**, but the transfer support layer may

also be provided in the vicinity of the gate electrode TX1 of the p-type semiconductor region **32**, in place of the electric field suppression layer **23**.

[0115] In addition, in the above described seventh embodiment, an example has been shown in which the electric field alleviation layer **23** is formed so as to extend to the lower region of the gate electrode TX1, but in the above described fifth embodiment as well, the electric field alleviation layer **24** may be formed so as to extend to the lower region of the gate electrode TX1. In addition, in the above described fifth embodiment, the electric field suppression layer **25** may also be formed so as to extend to the lower region of the gate electrode TX2.

[0116] In addition, the electric field suppression layer shown in the fifth embodiment and the auxiliary transfer layer shown in the sixth embodiment may be provided also in the vicinity of the gate electrode OFG of the p-type semiconductor region **32** which constitutes the photoelectric conversion portion **1**. In this case, these electric field suppression layer and transfer support layer may also be formed so as to extend to the lower region of the gate electrode OFG, similarly to the case of the seventh embodiment.

[0117] In addition, in the above described second embodiment, the gate electrode TX1 has been formed so as to extend to the upper part of the charge holding portion **3** in the solid-state imaging device of the first embodiment, but the gate electrode TX1 may be formed so as to extend to the upper part of the charge holding portion **3** also in the solid-state imaging devices of the third to seventh embodiments.

[0118] While the present invention has been described with reference to exemplary embodiments, it is to be understood that the invention is not limited to the disclosed exemplary embodiments. The scope of the following claims is to be accorded the broadest interpretation so as to encompass all such modifications and equivalent structures and functions.

[0119] This application claims the benefit of Japanese Patent Application No. 2014-051198, filed Mar. 14, 2014, and Japanese Patent Application No. 2014-164106, filed Aug. 12, 2014, which are hereby incorporated by reference herein in their entirety.

1.-28. (canceled)

29. An imaging device comprising:

- a first pixel and a second pixel, each of which includes:
 - a photoelectric conversion portion which photoelectrically converts incident light to generate a signal charge;
 - a charge holding portion that accumulates the signal charge transferred from the photoelectric conversion portion;
 - a floating diffusion region to which the signal charge of the charge holding portion is transferred;
 - a first transfer gate configured to transfer the signal charge from the photoelectric conversion portion to the charge holding portion; and
 - a second transfer gate configured to transfer the signal charge from the charge holding portion to the floating diffusion region,

wherein the photoelectric conversion portion includes a first semiconductor region of a first conductivity type, and a second semiconductor region of a second con-

ductivity type including a majority carrier of a polarity of the signal charge formed under the first semiconductor region,

wherein, in a planar view, the second semiconductor region of the first pixel and the second semiconductor region of the second pixel adjacent to the second semiconductor region of the first pixel are arranged along a first direction, and

wherein, in the planar view, the second transfer gate of the first pixel is arranged at a straight line through the floating diffusion region of the second pixel, the second transfer gate of the second pixel, and a portion of the charge holding portion of the second pixel.

30. The imaging device according to claim **29**, further comprising a third pixel and a fourth pixel each of which includes the photoelectric conversion portion, the charge holding portion, the floating diffusion region, the first transfer gate, and the second transfer gate,

wherein, in the planar view, the second semiconductor region of the third pixel and the second semiconductor region of the fourth pixel adjacent to the second semiconductor region of the third pixel are arranged along the first direction, the second semiconductor region of the first pixel and the second semiconductor region of the third pixel adjacent to the second semiconductor region of the first pixel are arranged along a second direction crossing the first direction, and the second semiconductor region of the second pixel and the second semiconductor region of the fourth pixel adjacent to the second semiconductor region of the second pixel are arranged along the second direction, and

wherein the floating diffusion region of the first pixel is arranged between the second semiconductor region of the second pixel and the second semiconductor region of the fourth pixel in the planar view.

31. The imaging device according to claim **30**,

wherein the first pixel further includes a reset transistor, and

wherein the reset transistor is arranged between the second semiconductor region of the second pixel and the second semiconductor region of the fourth pixel in the planar view.

32. The imaging device according to claim **30**, wherein the first transfer gate of the first pixel is arranged so that a longitudinal direction of the first transfer gate of the first pixel crosses the second direction.

33. The imaging device according to claim **30**, wherein the photoelectric conversion portion, the charge holding portion, and the first transfer gate of the first pixel are respectively arranged in translational symmetry with the photoelectric conversion portion, the charge holding portion, and the first transfer gate of the second pixel.

34. The imaging device according to claim **30**,

wherein the first pixel further includes a source follower transistor, and

wherein the source follower transistor is arranged so that a channel length direction of the source follower transistor crosses the second direction.

35. The imaging device according to claim **34**, wherein the channel length direction of the source follower transistor is parallel to the second direction.

36. The imaging device according to claim **30**, wherein the first pixel further includes a reset transistor, wherein the reset transistor is arranged so that a channel length direction of the reset transistor crosses the first direction.

37. The imaging device according to claim **36**, wherein the channel length direction of the reset transistor is parallel to the second direction.

38. An imaging device comprising:

a first pixel, a second pixel, a third pixel, and a fourth pixel, each of which includes:

a photoelectric conversion portion which photoelectrically converts incident light to generate a signal charge and includes a first semiconductor region of a first conductivity type, and a second semiconductor region of a second conductivity type including a majority carrier of a polarity of the signal charge formed under the first semiconductor region;

a charge holding portion that accumulates the signal charge transferred from the photoelectric conversion portion;

a floating diffusion region to which the signal charge of the charge holding portion is transferred;

a first transfer gate configured to transfer the signal charge from the photoelectric conversion portion to the charge holding portion; and

a second transfer gate configured to transfer the signal charge from the charge holding portion to the floating diffusion region,

wherein, in a planar view, the second semiconductor region of the first pixel and the second semiconductor region of the second pixel adjacent to the second semiconductor region of the first pixel are arranged along a first direction, the second semiconductor region of the third pixel and the second semiconductor region of the fourth pixel adjacent to the second semiconductor region of the third pixel are arranged along the first direction, the second semiconductor region of the first pixel and the second semiconductor region of the third pixel adjacent to the second semiconductor region of the first pixel are arranged along a second direction crossing the first direction, and the second semiconductor region of the second pixel and the second semiconductor region of the fourth pixel adjacent to the second semiconductor region of the second pixel are arranged along the second direction,

wherein, in the planar view, the floating diffusion region of the first pixel is arranged different region from the floating diffusion region of the third pixel, and

wherein, in the planar view, the floating diffusion region of the first pixel is arranged between the second semiconductor region of the second pixel and the second semiconductor region of the fourth pixel.

39. The imaging device according to claim **38**,

wherein the first pixel further includes a reset transistor, and

wherein the reset transistor is arranged between the second semiconductor region of the second pixel and the second semiconductor region of the fourth pixel in the planar view.

40. The imaging device according to claim **39**, wherein the first transfer gate of the first pixel is arranged so that a longitudinal direction of the first transfer gate of the first pixel crosses the second direction.

41. The imaging device according to claim **40**, wherein the photoelectric conversion portion, the charge holding

portion, and the first transfer gate of the first pixel are respectively arranged in translational symmetry with the photoelectric conversion portion, the charge holding portion, and the first transfer gate of the second pixel.

42. The imaging device according to claim **38**,

wherein the first pixel further includes a source follower transistor, and

wherein the source follower transistor is arranged so that a channel length direction of the source follower transistor crosses the second direction.

43. The imaging device according to claim **42**, wherein the channel length direction of the source follower transistor is parallel to the second direction.

44. The imaging device according to claim **39**, wherein the reset transistor is arranged so that a channel length direction of the reset transistor crosses the first direction.

45. The imaging device according to claim **44**, wherein the channel length direction of the reset transistor is parallel to the second direction.

46. An imaging device comprising:

a first pixel, a second pixel, a third pixel, and a fourth pixel, each of which includes:

a photoelectric conversion portion which photoelectrically converts incident light to generate a signal charge and includes a second semiconductor region of a second conductivity type including a majority carrier of a polarity of the signal charge;

a charge holding portion that accumulates the signal charge transferred from the photoelectric conversion portion;

a floating diffusion region to which the signal charge of the charge holding portion is transferred;

a first transfer gate configured to transfer the signal charge from the photoelectric conversion portion to the charge holding portion; and

a second transfer gate configured to transfer the signal charge from the charge holding portion to the floating diffusion region,

wherein the photoelectric conversion portion, the charge holding portion, and the floating diffusion region of the first pixel are arranged in a first active region,

wherein the photoelectric conversion portion, the charge holding portion, and the floating diffusion region of the second pixel are arranged in a second active region,

wherein the photoelectric conversion portion, the charge holding portion, and the floating diffusion region of the third pixel are arranged in a third active region,

wherein the photoelectric conversion portion, the charge holding portion, and the floating diffusion region of the fourth pixel are arranged in a fourth active region,

wherein each of the first active region, the second active region, the third active region, and the fourth active region are separated respectively,

wherein, in a planar view, the first active region and the second active region are arranged along a first direction, the third active region and the fourth active region are arranged along the first direction, and the first active region and the fourth active region are arranged along a second direction crossing the first direction, and

wherein, in the planar view, a part of the first active region is arranged between the third active region and the fourth active region.

47. The imaging device according to claim **46**,

wherein the first active region includes a reset transistor, and

wherein the reset transistor is arranged between the third active region and the fourth active region in the planar view.

48. The imaging device according to claim **47**, wherein the first transfer gate of the first pixel is arranged so that a longitudinal direction of the first transfer gate of the first pixel crosses the second direction.

49. The imaging device according to claim **48**, wherein the photoelectric conversion portion, the charge holding portion, and the first transfer gate of the first pixel are respectively arranged in translational symmetry with the photoelectric conversion portion, the charge holding portion, and the first transfer gate of the second pixel.

50. The imaging device according to claim **46**,

wherein the first active region includes a source follower transistor, and

wherein the source follower transistor is arranged so that a channel length direction of the source follower transistor crosses the second direction.

51. The imaging device according to claim **50**, wherein the channel length direction of the source follower transistor is parallel to the second direction.

52. The imaging device according to claim **47**, wherein the reset transistor is arranged so that a channel length direction of the reset transistor crosses the first direction.

53. The imaging device according to claim **52**, wherein the channel length direction of the reset transistor is parallel to the second direction.

* * * * *